

Notice of References Cited	Application/Control No. 10/800,653	Applicant(s)/Patent Under Reexamination SU ET AL.	
	Examiner Aristocratis Fotakis	Art Unit 2611	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-7,069,481	06-2006	Lee et al.	714/707
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	M.-J Edward Lee, William J. Dally, John W. Poulton, Patrick Chiang, Stephen F. Greenwood, An 84-mW 4-Gb/s Clock and Data Recovery Circuit for Serial Link Applications, VLSI Circuits Symposium, Kyoto, Japan, June 2001
	V	Dong-Hee Kim, Jin-Ku Kang, Clock and data recovery circuit with two exclusive-OR phase frequency detector, Electronic Letters, Vol.36, No.16, 1347-1349, 3rd August 2000
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.